Hall Ticket Number:

Code No. : 13664 N/O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (I.T.) III-Semester Main & Backlog Examinations, Jan./Feb.-2024

Digital Electronics and Logic Design

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Convert the following numbers into decimal a. $(4310)_5$ b. $(198)_{12}$	2	1	1	1
2.	If $(14)_x = 7$ in a particular number system, determine the base of the number system.	2	1	1	1
3.	Draw the logic circuit diagram of a 2 x 1 Multiplexer.	2	2	2	1
4.	Derive the truth table of a full adder circuit.	2	1	2	1
5.	Draw the circuit diagram of a JK flip flop.	2	2	3	1
6.	What is the need for Master-Slave flipflops?	2	1	3	1
7.	List the basic design steps for synchronous sequential circuit.	2	1	4	1
8.	What is state equivalence principle?	2	1	4	1
9.	What is VHDL?	2	1	5	1
10.	Give the importance of Process keyword and the sensitivity list of the process keyword used in VHDL.	2	1	5	1
	Part-B (5 × 8 = 40 Marks)				
11. a)	Given two binary numbers X=1010100 Y=1000011 perform the subtraction X-Y and Y-X by using 2's complements.	4	2	1	1
b)	Simplify the Boolean function $F(w,x,y,z) = \Sigma(1,3,7,11,15)$ which has the don't care conditions $d(w,x,y,z) = \Sigma(0,2,5)$	4	2	1	1
12. a)	Implement the Boolean functions F1= AB' + AC + A'BC' and F2 = (AC + BC)' using a Programmable logic array (PLA).	4	3	2	3
b)	Implement the Boolean function $F(A,B,C,D) = \Sigma(1,3,4,11,12,13,14,15)$ using a multiplexer by considering A,B,C as selection lines of the multiplexer.	4	3	2	3
13. a)	What is characteristic equation of a flip flop? Derive the characteristic equation of a J K flip flop.	4	2	3	2
b)	Convert a JK flip flop to a T flip flop.	4	2	3	2

Contd... 2

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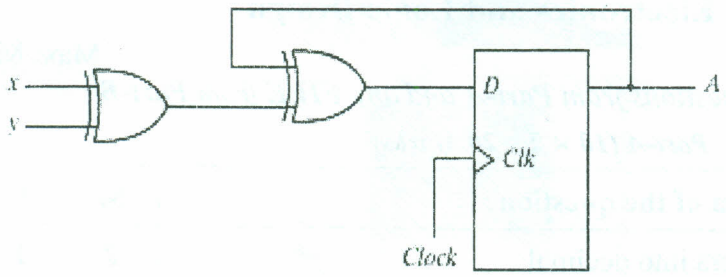
14. a)	Analyze the following clocked sequential circuit shown below: 	4	3	4	2
b)	Distinguish between Mealy and Moore Finite State Machines.	4	2	4	1
15. a)	Explain the different types of hazards and explain how they can be overcome.	4	3	4	1
b)	Describe the components of an ASM charts and explain the usage of ASM charts with an example.	4	2	4	1
16. a)	Express the Boolean function F1 = A +B'C as sum of min terms and the Boolean function F2= xy + x'z as product of max terms.	4	3	1	1
b)	Write the VHDL code for a 2 X 1 Multiplexer.	4	3	5	3
17.	Answer any ***two*** of the following:				
a)	Draw the logic circuit diagram of an SR latch constructed using NOR gates and explain its operation.	4	3	3	2
b)	Design a synchronous modulo -6 counter using T flipflops.	4	3	4	3
c)	Write the VHDL code for a positive edge triggered D flip flop.	4	4	5	3

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	35%
iii)	Blooms Taxonomy Level – 3 & 4	45%

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